<u>**REMARKS**</u>

Claims 1-37 remain pending in the present application. Claims 35-37 were amended solely to correct a typographical error. In the Office Action, claims 1-2, 4-9, 11-14, 16-19, 21, 23-25, 27-29, 31-34, and 36-37 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Maruyama (U.S. Patent No. 6,052,763). The Examiner's rejections are respectfully traversed.

With regard to independent claims 1, 11-13, 23, and 32, Applicants describe and claim a memory management unit for managing a memory storing data arranged within a plurality of memory pages, and a method for providing access security for a memory. The memory management unit includes a security check unit coupled <u>to receive a physical address</u> generated during execution of a current instruction. The claimed physical address resides within a selected memory page. The security check unit is configured to use the physical address to access at least one security attribute data structure located in the memory to obtain a security attribute of the selected memory page, to <u>compare a numerical value conveyed by a security attribute of the current instruction to a numerical value conveyed by the security attribute of the selected memory page</u>, and to produce an output signal dependent upon a result of the comparison. The memory management unit is configured to access the selected memory page dependent upon the output signal.

Maruyama is directed to a memory unit and a method for coordinating atomic memory transactions in a tightly coupled multiprocessor system. Maruyama describes a system bus 15 and a system bus interface 16 coupled to a decoder 21, a register 22, a comparator 23, and a master ID table 24. See Maruyama, Figure 4. The system bus 15 and the system bus interface 16 provide <u>an access address</u> to the decoder 21, which identifies whether the access address is for a

conventional address space or for an atomic address space. See Maruyama, col. 6, ll. 11-15. The system bus 15 and the system bus interface 16 also provide <u>a bus master ID</u> to the register 22, the comparator 23, and the master ID table 24. See Maruyama, col. 6, ll. 44-47. In an atomic transaction mode, an ID of the bus master that is making the atomic transaction request is temporally stored in the register 22. Subsequently, the comparator 23 <u>compares the temporally stored bus master ID with the ID of the requesting device.</u> See Maruyama, col. 7, ll. 26-34. The master ID table 24 uses the bus master ID to distinguish whether or not a bus master is a processor. See Maruyama, col. 6, ll. 47-50.

The Examiner alleges that the comparator 23 receives <u>an access address</u> and uses a bus master ID table as an identifier to determine if the requesting processor is a bus master with privileges for performing a transaction. Applicants respectfully disagree and submit that, as noted above, the comparator 23 receives <u>a bus master ID,</u> and not <u>an access address.</u> Furthermore, Applicants respectfully submit that the comparator 23 does not access the bus master ID table 24 to obtain <u>a bus master ID.</u> As stated above, the system bus 15 and the system bus interface 16 provide <u>the bus master ID</u> to the comparator 23.

The Examiner also alleges that the comparator 23 <u>compares the bus master ID with a bus master ID from the master ID table 24</u> and then outputs an error signal if the bus master ID does not match. Applicants respectfully disagree. As stated above, the comparator 23 <u>compares the bus master ID that is temporally stored in register 22 with the ID of the requesting device that is provided by the system bus interface 16.</u> Moreover, as also stated above, the master ID table 24 uses the bus master ID (provided by the system bus interface 16) to distinguish whether or not a bus master is a processor.

For at least the aforementioned reasons, Applicants respectfully submit that independent claims 1, 11-13, 23, 32, and all claims depending therefrom are not anticipated by Maruyama and request that the Examiner's rejections of these claims under 35 U.S.C. 102(b) be withdrawn.

In the Office Action, claims 10, 20, 22, 26, and 35 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Maruyama in view of Applicants' admitted prior art. The Examiner's rejections are respectfully traversed.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) <u>must teach or suggest all the claim limitations</u>. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Claims 10, 20, 22, 26, and 35 depend from independent claims 1, 13, 23, and 32. As discussed above, Maruyama fails to teach or suggest many aspects of the present invention set forth in independent claims 1, 13, 23, and 32. The Examiner relies on the admitted prior art to teach use of a user/supervisor bit and/or a read/write bit. However, Applicants respectfully submit that the admitted prior art does not remedy the fundamental deficiencies of the primary reference. Thus, Applicants respectfully submit that claims 10, 20, 22, 26, and 35 are not obvious over Maruyama in view of the admitted prior art and request that the Examiner's rejections of these claims under 35 U.S.C. 103(a) be withdrawn.
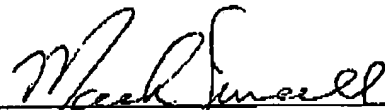
In the Office Action, claims 1-37 were provisionally rejected under 35 USC 101 for allegedly claiming the same invention as that of claims 1-37 of co-pending Application Number 10/010,161. However, the Examiner admits at item 7 on page 5 of the Office Action that the conflicting claims are not identical. Thus, Applicants respectfully submit that, by the Examiner's own admission, claims 1-37 of the present application and claims 1-37 of co-pending Application Number 10/010,161 do not claim the same invention, and therefore the Examiner's

provisional rejection of claims 1-37 is improper. Applicants respectfully request that the Examiner's provisional rejection of these claims under 35 USC 101 be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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Mark W. Sincell, Ph.D.
Reg. No. 52,226
Williams Morgan & Amerson, P.C.
10333 Richmond Avenue, Suite 1100
Houston, TX 77042
(713) 934-7000
(713) 934-7011 (Fax)

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